

Task 6.1: Modeling of Ge / InGaAs FinFETs

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Move towards 3D FinFETs

CMOS SCALING - INNOVATIONS IN PAST DECADE

Source: www.intel.com

2003: 90 nm
2005: 65 nm
2007: 45 nm
2009: 32 nm
2011: 22 nm

Move towards 3D structures

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Next Move - High μ channel materials

Source: ITRS

Structure (electrostatic control)

ITRS predicts high μ channel materials \rightarrow Ge / InGaAs by 2016

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InGaAs FinFETs - Experiments

p-type (100) InP substrate
Undercut etching
(100) wafer
Source, EXT, p-InGaAs Fin-Channel, Drain, p+ InP
Experimental structure

- IEDM 2011 (Prof. Ye group, Purdue)
- Fabricated $<100>$ In_{0.53}Ga_{0.47}As NMOS FinFET, Lg=50nm
- Gate all around structure.
- Two different Fin widths studied : H_{Fin}=30 nm & W_{Fin}=30 nm / 50 nm

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InGaAs FinFETs - Experiments

EOT=4.5nm
H_{Fin}=30nm
W_{Fin}=30nm
Expt. W=50nm
Increasing current observed in experiments with decreasing Fin width (W_{Fin})

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InGaAs FinFETs - Simulation

E-k calculation using sp3s* tight-binding model for In_{0.53}Ga_{0.47}As (NEMO5)
 $\tau_{SR}(E) \propto E_{eff}^2 \propto Q_{inv}^2$
D_t=5.6e12 eV.cm²
H=30nm W=30nm
H=30nm W=50nm

- Bandstructure calculations performed for the two experimental cases.
- Computed non-self consistent Top-of-the-barrier Id-Vg including trap density (Expt.) and back-scattering effect due to surface roughness.
- Initial assessment \rightarrow For W=30nm \rightarrow increased separation of bands \rightarrow reduced DOS(E) \rightarrow reduced scattering \rightarrow Higher I_{ON}

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Ge FinFETs for PMOS – motivation

Si	Ge	InP	InAs	InSb		
Electron mob. (cm ² /Vs)	1600	3900	9200	5400	40,000	77,000
Electron mass m _e /m ₀	0.19	0.082	0.067	0.082	0.023	0.014
Hole mob. (cm ² /Vs)	430	1900	400	200	500	850
Band gap (eV)	1.12	0.66	1.42	1.34	0.36	0.17
Permittivity	11.8	16	12	12.6	14.8	1

Highest hole mobility in Ge
FinFET structures
High performance PMOS device

(100) wafer

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Ge FinFET – device optimization

(1) Effect of uniaxial compressive strain
(2) Effect of surface / transport orientation
(3) Effect of Fin width scaling

Modeling of Ge FinFETs by exploring the effect of strain/orientation/and Fin width scaling, aimed at Lg=14 nm.

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Effect of orientation : comparison with expt.

Self-consistent Top of the barrier model (NEMO5)
Injection velocity (cm/s) vs mobility (cm²/V-s)
(110)/<110> vs (100)/<100>
Normalized charge contour plots

- Similar enhancement in hole injection velocity and mobility at the same inversion charge = 1e13/cm² in Ge FinFET (H=8nm, W=6.6nm)
- Injection velocity a good performance metric

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(100)/<100> : Effect of strain/Fin width

Self consistent E-k at Qinv~1e13/cm²
W=2.1nm 0 GPa m=0.016
W=6.6nm 0 GPa m=0.019
W=2.1nm -1.8 GPa m=0.014
W=6.6nm -1.8 GPa m=0.015
Energy (eV) vs k_x (1/a₀)
H (nm) vs W (nm)
Energy (eV) vs k_x (1/a₀)
H (nm) vs W (nm)
Energy (eV) vs k_x (1/a₀)
H (nm) vs W (nm)
Energy (eV) vs k_x (1/a₀)
H (nm) vs W (nm)

- Decreasing mass at VB top with strain
- Decreasing mass at VB top with Fin width reduction.

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(110)/<110> : Effect of strain/Fin width

Self consistent E-k at Qinv~1e13/cm²
W=2.1nm 0 GPa m=0.016
W=6.6nm 0 GPa m=0.019
W=2.1nm -1.8 GPa m=0.014
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Injection velocity – (100) vs (110)

V_{inj} computed at Q_{inv}=1e13/cm²
(100)/<100> vs (110)/<110>
Fin width (nm) vs Uniaxial strain (-GPa)
Fin width (nm) vs W (nm)

- (110)/<110> orientation has ~ 2.5x higher v_{injection} than (100)/<100> orientation at all conditions.
- Fin width scaling further improves performance in (110)/<110> unlike (100)/<100>.

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Conclusions and Future Work

- InGaAs and Ge nFinFETs material systems relevant for next generation MOSFETs.
- InGaAs nFinFET exhibits improvement with Fin width scaling \rightarrow Increased quantization \rightarrow reduced DOS \rightarrow reduced scattering \rightarrow Better performance.
- (110)/<110> oriented Ge pFinFET showed to be better than (100)/<100>.
- Fin width scaling along (110) identified as a performance booster that is additive to enhancements due to strain in Ge pFinFETs.

FUTURE WORK

- Self consistent simulations for InGaAs FinFETs including strain and extract ballistic Id-Vg.
- Explore device designs with SiGe channel for pFinFET

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